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S.Y. B.Sc.

ELECTRONIC SCIENCE

EL-212 : Digital Circuit Design

(2013 Pattern) (Paper - II) (Semester-I)

Time : 2 Hour] ***[Max. Marks : 40***

Instructions to the candidates:

1) ***All questions are compulsory.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicate full marks.***

Q1) Answer All of the following:

a) Write excitation table for J-K flipflop. **[1]**

b) What is steady state accuracy test for digital to analog converter? **[1]**

c) What do you mean by octet in K-map? **[1]**

d) State the nature of input and output in case of thumb wheel switch. **[1]**

e) Draw K-map for following equation

$Y = A\overline{B}C + \overline{A}\overline{B}C + \overline{A}BC + A\overline{B}\overline{C} + \overline{A}\overline{B}\overline{C}$. **[2]**

f) "Non multiplexed display system draws large current from the power supply". Comment. **[2]**

g) "Flash type ADC is fastest ADC". Comment. **[2]**

h) State various methods for sequence generator. **[2]**

Q2) Attempt any Two of the following:

a) Using K- map design 3-bit odd parity generator. **[4]**

b) With the help of diagram explain the working of counter type ADC. **[4]**

c) Draw a logic diagram and timing diagram of asynchronous decade counter using J-K flipflop. **[4]**

P.T.O.

Q3) Attempt any Two of the following:

a) What are limitations of binary weighted resistire DAC? How is it overcome in R-2R ladder network? **[4]**

b) Design a full adder circuit using K-map. **[4]**

c) Draw block diagram of digital clock and explain second counter in detail. **[4]**

Q4) Attempt All of the following:

a) With the help of block diagram explain in detail auto parking system. **[6]**

b) Draw state table and state diagram of a sequential circuit described algebrically by following state equations. **[6]**

Output $Z = X(t) \cdot Q_1(t)$

$$Q_1(t+1) = X(t) + Q_1(t)$$

$$Q_2(t+1) = X(t) \cdot \overline{Q_2}(t) + \overline{X}(t) \cdot \overline{Q_1}(t)$$

OR

a) Find the output voltage from a 5 - bit R - 2R ladder network for digital input 11010, given input voltage levels are O=0v & 1=10v. **[4]**

b) Design a onebit magnitude comparator using K-map. **[4]**

c) Design a counter using J-K flipflop for the sequence 1, 2, 3, 1, 2-----. **[4]**