Total No. of Questions—**8**] [Total No. of Printed Pages—**2**

Seat No.	

[5668]-203

S.E. (Information Technology) (I Semester) EXAMINATION, 2019
DIGITAL ELECTRONICS AND LOGIC DESIGN
(2015 PATTERN)

Time : Two Hours **Maximum Marks : 50**

N.B. **:—** (*i*) Answer Q. Nos. **1** or **2**, **3** or **4**, **5** or **6**, **7** or **8**.
(*ii*) Neat diagrams must be drawn wherever necessary.
(*ii*) Figures to the right indicate full marks.
(*iii*) Assume suitable data, if necessary.

1. (*a*) Convert the following octal number into its equivalent Binary Decimal and Hexadecimal $(357.3)_8$. [6]

(*b*) Design and draw four bit Excess-3 adder using IC 7483. [6]

Or

2. (*a*) What is Logic Family ? Explain the terms : [6]
(*i*) Fan out
(*ii*) Propagation Delay.

(*b*) Design Full Adder using IC 74153. [6]

3. (*a*) Compare combinational circuits with sequential circuits. Convert JK Flip-Flop into SR flip-flop. [6]

(*b*) Draw 3-bit Ring and Twisted ring counter. Draw state diagram for 3-bit Ring and Twisted ring counter, assuming initial state as 001. [7]

Or

4. (*a*) Design 3-bit Synchronous up counter with JK flip-flops. [6]

(*b*) Design a sequence generator to generate the following sequence 10101 using JK flip-flop. [7]

P.T.O.

5. (*a*) Explain the difference between CPLD and FPGA. [6]

(*b*) Draw ASM chart for 2-bit binary down counter having one enable line such that : E = 1 (Counting enabled), E = 0 (Counting disabled). [6]

Or

6. (*a*) Implement the following function using PLA : [6]
$F_1(A, B, C) = \Sigma m(0, 2, 5, 6)$ $F_2(A, B, C) = \Sigma m(1, 4, 5, 6)$.

(*b*) Design and implement 3-bit gray to binary code converter using PAL. [6]

7. (*a*) State and explain any *three* data types supported by VHDL. [6]

(*b*) Explain he process statement in behavior model of VHDL with respect to syntax, sensitivity list and declarative part. [7]

Or

8. (*a*) What is Structural Modeling ? Implement full Adder using Structural Modeling. [6]

(*b*) What is VHDL ? Explain entity-architecture declaration for 2-bit NAND and OR gate. [7]