May - June - 2011

Total No. of Questions—12] [Total No. of Printed Pages—4

[3962]-203

S.E. (Comp. Engg.) (I Sem.) EXAMINATION, 2011

(Common to I.T.)

DIGITAL ELECTRONICS AND LOGIC DESIGN

(2008 PATTERN)

Time : Three Hours **Maximum Marks : 100**

N.B. :— (*i*) Answer Questions **1** or **2**, **3** or **4**, **5** or **6** from Section I and Questions **7** or **8**, **9** or **10**, **11** or **12** from Section II.

(*ii*) Answers to the two sections should be written in separate answer-books.

(*iii*) Neat diagrams must be drawn wherever necessary.

(*iv*) Figures to the right indicate full marks.

(*v*) Assume suitable data, if necessary.

SECTION I

1. (*a*) For a maximum 3-digit octal number obtain equivalent hex, binary, decimal number. [3]

(*b*) Perform the following operation and show your answer in hexadecimal, decimal and octal format : [15]

(*i*) $(7FF)_{Hex} - (777)_{Octal}$

(*ii*) $(2078)_{Decimal} - (3FF)_{Hex}$

P.T.O.

(*iii*) $(1111)_{Decimal} - (1111)_{Binary}$

(*iv*) $(3258)_{Octal} + (FFF)_{Hex}$

(*v*) $(1110)_{Binary} + (1110)_{Decimal}$

Or

2. (*a*) Design and explain in detail 4-bit grey code to 5-bit BCD code conversion. For this design use K-map reduction and MSI circuit using basic gates. [16]

(*b*) Explain rule for any sequence binary to grey code conversion. [2]

3. (*a*) Draw and explain 3-i/p TTL NAND gate circuit, also write various i/p, o/p states with transistor ON/OFF condition. [10]

(*b*) Explain OR Gate using CMOS logic. [6]

Or

4. (*a*) Solve the following reduction using K-map, also draw MSI circuit for the output : [12]

(*i*) $Z = f(A, B, C, D) = \Sigma(1, 2, 7, 8, 10, 12, 15) + d(0, 5, 6)$

(*ii*) $Z = f(A, B, C, D) = \Sigma(1, 3, 4, 6, 8, 11, 15) + d(0, 5, 7)$

(*b*) Explain various characteristics for TTL logic families. [4]

5. (*a*) Explain 16 : 1 mux using 4 : 1 mux in detail with necessary diagram. [8]

(*b*) Explain decoder (1 : 8) as a binary to grey code converter. Show your design. [8]

Or

6. (*a*) Draw and explain 4-bit BCD adder using IC 7483. Also explain with example addition of numbers with carry. [8]

(*b*) Explain working of cascaded mode IC 7485 magnitude comparator. [8]

SECTION II

7. (*a*) Draw 4-bit Asynchronous Counter. Also explain timing diagram for the same. [8]

(*b*) What is advantage of MOD counter ? Explain working of MOD-27 and MOD-13 counter with detail diagram. [10]

Or

8. (*a*) What is S-R flip-flop ? Explain working of clocked SR flip-flop. What is edge triggering ? [10]

(*b*) Explain ring counter design for the initial condition '10110', also explain twisted ring counter in biref. [8]

9. (*a*) What is VHDL ? Explain entity-architecture declaration for universal gates. [8]

(*b*) What is ASM chart ? Design ASM chart for 3-bit octal number sequence with up-down conditions. [8]

Or

10. (*a*) What is ASM chart ? Explain the MUX controller method with suitable example. [8]

(*b*) Draw an ASM chart and state table for a sequential ring counter with suitable present state and conditional input. [8]

11. (*a*) Explain execution sequence of a sample program.

[Hint : Assume basic microprocessor instructions]. [8]

(*b*) Explain the design model of PAL. [8]

Or

12. (*a*) Explain in brief, for performing the various operations, a basic microprocessor must consist of what various blocks ? [8]

(*b*) Explain in brief interfacing of memory with microprocessor.

[Hint : Assume 16-bit address bus and 8-bit data bus] [8]