Total No. of Questions—**12**] [Total No. of Printed Pages—**4+1**

Seat No.	

[4657]-81

S.E. (Information Technology) (First Semester) EXAMINATION, 2014

COMPUTER ORGANIZATION

(2008 PATTERN)

Time : Three Hours **Maximum Marks : 100**

N.B. **:—** (*i*) Answer Q. No. **1** *or* Q. No. **2**, Q. No. **3** *or* Q. No. **4**, Q. No. **5** *or* Q. No. **6** from Section I and Q. No. **7** *or* Q. No. **8**, Q. No. **9** *or* Q. No. **10**, Q. No. **11** *or* Q. No. **12** from Section II.

(*ii*) Answers to the two Sections should be written in separate answer-books.

(*iii*) Neat diagrams must be drawn wherever necessary.

(*iv*) Figures to the right indicate full marks.

(*v*) Assume suitable data, if necessary.

SECTION I

1. (*a*) Compare Restoring and Non-Restoring division algorithm. Divide the following numbers using restoring division algorithm and justify your answer :

Dividend = $(21)_{10}$; Divisor = $(03)_{10}$. [10]

P.T.O.

(*b*) Draw IEEE standards for single precision and double precision floating point numbers. Represent $(-84.25)_{10}$ in single precision and double precision format. [8]

Or

2. (*a*) Explain Booth's algorithm to multiply the following pair of numbers : [10]

Multiplicand = $(15)_{10}$ multiplier = $(-6)_{10}$.

(*b*) Draw IAS (Von Neumann) Architecture and explain function of registers in it. [8]

3. (*a*) State design factors in design of instruction format. Draw instruction format for INTEL Processor and explain various fields in it. [8]

(*b*) Explain with examples the following addressing modes of 8086 : [8]

(*i*) Immediate addressing mode

(*ii*) Register indirect addressing mode

(*iii*) Base index with displacement

(*iv*) Direct addressing mode.

Or

4. (*a*) Draw timing diagram for memory read cycle of 8086 in Minimum Mode and list operations in each T state. [8]

(*b*) Write a note on MAX/MIN mode of 8086. [8]

5. (*a*) Draw and explain single bus organization of the CPU, showing all the registers and data paths. [8]

(*b*) Explain design of multiplier control unit using delay element method. [8]

Or

6. (*a*) Explain the sequence of operations needed to perform processor functions : [8]

(*i*) Fetching a word from memory

(*ii*) Performing an arithmetic or logical operation.

(*b*) Compare :

(*i*) Horizontal and vertical microinstruction representation

(*ii*) Hardwired and microprogrammed control unit. [8]

SECTION II

7. (*a*) What is cache coherence and discuss MESI protocol ? [8]

(*b*) Discuss set associative and fully associative cache mapping techniques with respect to mapping function, address structure, merits and demerits. [10]

Or

8. (*a*) What is virtual memory ? Explain address translation mechanism for converting virtual address into physical address with neat diagram. [10]

(*b*) Write short notes on (any *two*) : [8]

(1) SRAM

(2) DVD

(3) RAID

(4) EEPROM.

9. (*a*) What is DMA ? Explain DMA operation with a diagram. Also explain data transfer modes in DMA. [8]

(*b*) Compare : [8]

(*i*) Memory mapped I/O and I/O mapped I/O

(*ii*) Programmed I/O and interrupt driven I/O.

Or

10. (*a*) List the features of IC 8255 and IC 8251. [8]

(*b*) Explain the working principle of the following : [8]

(1) Laser printer

(2) Video displays.

11. (*a*) Compare closely coupled and loosely coupled multiprocessor configurations. Explain loosely coupled multiprocessor configuration. [10]

(*b*) What is cluster ? State the advantages of clustering. [6]

Or

12. (*a*) Compare the following : [8]

(*i*) RISC and CISC

(*ii*) UMA and NUMA.

(*b*) Explain briefly : [8]

(*i*) Instruction level pipelining

(*ii*) Superscalar architecture.