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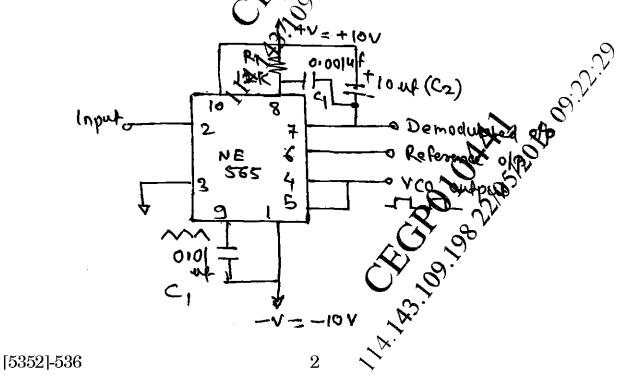
Total No. of Questions—8] [Total No. of Printed Pages—3		
Seat No.	[5352]-536	
	.E. (Electron (II Sem.) EXAMINATION, 2018 INTEGRATED CIRCUITS (2015 PATTERN)	
	(2015 PATTERN)	
Time : T	Maximum Marks: 50	
<i>N.B.</i> :—	(i) Answer Q. No. 1 or Q. No. 2, Q. No. 3 or Q. No. 4,	
	Q. No. 5 or Q. No. 6, Q. No. 7 or Q. No. 8.	
	(ii) Neat diagrams must be drawn wherever necessary.	
	(iii) Figures to the right indicate full marks.	
	(iv) Your answers will be valued as a whole.	
	(v) Assume suitable data, if necessary.	
1. (a)	Explain the following op-amp parameters: [6]	
	(i) Input offset voltage	
	O.:	
	(iii) Slew Rate.	
(<i>b</i>)	Design a practical integrator for to operate at = 4 kHz	
	(iii) Slew Rate. Design a practical integrator for to operate at $P = 4$ kHz and gain is equal to 2. Draw equivalent circuit of op-amp with its ideal transfer curve.	
	Or Or	
2 . (a)	Draw equivalent circuit of op-amp with its ideal transfer	
	Draw equivalent circuit of op-amp with its ideal transfer curve.	
	P.T.O.	

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- (b) Draw the circuit diagram of practical differentiator and write equation for output voltage (V_o). [6]
- 3. (a) Draw circuit diagram and its input and output waveform for peak detector. [6]
 - (b) Draw creuit diagram for R-2R ladder DAC and write its output equation [6]
- 4. (a) Write short note on characteristic of comparator. [6]

Or

- (b) Draw circuit diagram of Binary weighted DAC and write its output equation. [6]
- 5. (a) Calculate free running frequency F_{out} , the lock range F_t and the capture range F_c for the given circuit. [7]



	(b)	Explain the working principle of oscillator with the help of
		its block diagram. [6] Or Draw circuit diagram of frequency multiplier using PLL and
		\mathcal{O}^{X} \mathcal{O}^{Y} \mathcal{O}^{P}
6.	(a)	Draw credit diagram of frequency multiplier using PLL and
		explain its operation. [7]
	(b)	Draw circuit diagram of phase shift oscillator and explain its
		operation. [6]
7 .	(a)	Design a first order low pass filter with high cut-off frequency
		of 1 kHz and pass band gain is 3 Braw the circuit diagram with its component values [7]
		with its component values [7]
	(b)	with its component values. [7] Draw circuit diagram of second order high pass filter. [6]
8.	(a)	Design a first order high pass filter with low cut-off frequency
		of 6 kHz with pess band gain is 2. Draw the circuit diagram
		with its component values. [7]
	(<i>b</i>)	Draw circuit diagram of second order low pass filter. [6]
		with its component values. [7] Draw circuit diagram of second order low pass filter. [6]
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