

S.E. E & TC, Sem-II
 NOV-DEC 2012, 2008 pattern

Total No. of Questions—12]

[Total No. of Printed Pages—4+2

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S.E. (E&TC) (Second Semester) EXAMINATION, 2012

INTEGRATED CIRCUITS AND APPLICATIONS

(2008 PATTERN)

Time : Three Hours

Maximum Marks : 100

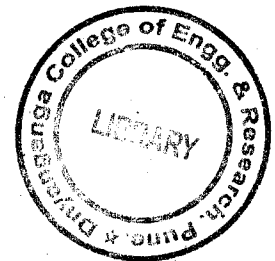
N.B. :— (i) Answer any *three* questions from each Section.

(ii) Answers to the two Sections should be written in separate answer-sheets.

(iii) Neat diagrams must be drawn wherever necessary.

(iv) Figures to the right indicate full marks.

(v) Assume suitable data, if necessary.



SECTION I

1. (a) Which are the different configurations of differential amplifiers ? Derive the expressions for Q-point parameters of Dual-Input balanced output differential amplifier. [8]

(b) The dual-input balanced output differential amplifier has the following specifications : [8]

$$R_c = 2.5 \text{ k}\Omega, R_E = 4.8 \text{ k}\Omega, R_{b1} = R_{b2} = R_b = 50 \text{ }\Omega, +V_{cc} = +10 \text{ V}, -V_{EE} = -10 \text{ V}, \beta = 100, V_{BE} = 0.8 \text{ V}.$$

P.T.O.

Assume $h_{ie} = 1.1 \text{ k}\Omega$.

Calculate :

- (1) Q-point values
- (2) Voltage gain
- (3) Input and output resistance.

Or

2. (a) Explain any *two* level shifter circuits used in op-amp used to shift the level. [6]
- (b) Write short notes on : [10]
 - (1) Current Mirror
 - (2) Widlar Current Source.

- 3 (a) An Op-Amp has a slew rate of $5 \text{ V}/\mu\text{s}$. Find the rise time for an o/p voltage of 10 V amplitude resulting from a rectangular pulse input if the op-amp is slew-rate limited [6]
- (b) Define the following characteristics of an Op-Amp :
 - (1) CMRR
 - (2) Input bias current
 - (3) Slew rate
 - (4) Input offset voltage. [4]

- (c) Explain the effect of feedback on closed loop stability of op-amp. [6]

Or

4. (a) Explain different types of noises associated with op-amp. Draw noise model of op-amp and give expression for noise voltage. [8]
- (b) What is the need of frequency compensation ? Explain any two methods of frequency compensation. [8]

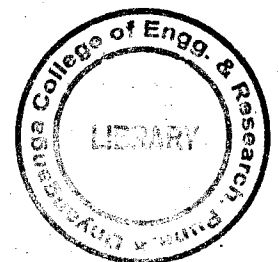
5. (a) Design a practical integrator using Op-Amp IC741C to satisfy the following specifications :

Assume $V_{cc} = +15$ V.

- (1) 3-dB cut-off frequency = 1.5 kHz
(2) D.C. gain = 10

Sketch the frequency response of the circuit. [8]

- (b) Explain grounded load V to I converter with necessary derivation. [6]
- (c) Explain the concept of defined non-linearity. [4]



Or

6. (a) Design a practical differentiator to differentiate an input signal that varies in frequency from 10 Hz to 500 Hz. Draw its frequency response. [8]
- (b) Compare the salient features of an integrator and differentiator using Op-Amp. [4]
- (c) Draw a neat diagram of three inputs inverting summing amplifier using op-amp and obtain expression for output voltage. [6]

SECTION II

7. (a) Explain the operation of inverting comparator with appropriate output waveforms. [6]
- (b) Explain peak detector using op-amp. [6]
- (c) Design an inverting Schmitt Trigger circuit whose V_{UT} and V_{LT} are $\pm 5V$. Draw input and output waveforms. Assume op-amp saturates at $\pm 13.5 V$. [6]

Or

8. (a) Explain the requirements of an instrumentation amplifier. [4]
- (b) Derive the output voltage of 3 op-amp instrumentation amplifier. [6]
- (c) Explain the operation of precision full wave rectifier with necessary waveforms. [8]

9. (a) Explain the following with reference to DAC : [6]
- (1) Linearity
 - (2) Accuracy
 - (3) Settling time.
- (b) Draw the circuit diagram of voltage mode R-2R ladder DAC and explain its working. [6]
- (c) List various specifications of ADC. [4]



Or

10. (a) With the help of neat circuit diagram, explain the operation of Dual Slope ADC. [8]
- (b) Draw the neat diagram of F to V converter and explain its operation. [8]
11. (a) Explain the operation of PLL using a neat block diagram. Define the terms Centre frequency and capture time related to PLL. [8]
- (b) Write short notes on : [8]
- (1) Graphic equalizer
 - (2) Frequency synthesizer using PLL.

Or

12. (a) Calculate output frequency f_o , lock range and capture range of PLL if the timing parameters are $C_T = 0.1 \mu\text{f}$, $R_T = 1 \text{ k}\Omega$. The filter capacitor is $10 \mu\text{f}$. [6]
- (b) Write a short note on Sallen and Key second order active low pass filter. [6]
- (c) Compare active and passive filters. [4]



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