Total No. of Questions : 4] **SEAT No. :**

P772 **[Total No. of Pages : 2**

[5315] - 361

T.Y.B.Sc.

ELECTRONIC SCIENCE

EL-331 - ADVANCED DIGITAL SYSTEM DESIGN

(2013 Pattern) (Semester - III) (Paper - I)

Time : 2 Hours] ***[Max. Marks : 40***

Instructions to the candidates:

1) ***All questions are compulsory.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicate full marks.***

Q1) Attempt all of the following.

a) List different variables used for state machine. **[1]**

b) Write the role of input buffers in PLA. **[1]**

c) What is meaning of 'forever' loop used in verilog? **[1]**

d) List components of a verilog module. **[1]**

e) Write two advantages of ASIC. **[2]**

f) What is concatenation operator? **[2]**

g) List four advantages of PLD. **[2]**

h) List four data types used in verilog. **[2]**

Q2) Attempt any two of the following.

a) Write a program in verilog for 4 bit full adder using data flow operators. **[4]**

b) Explain 'for' loop in verilog with suitable example. **[4]**

c) Compare synchronous and asynchronous sequential machines. **[4]**

Q3) Attempt any two of the following.

a) Write various symbols used in ASM diagram and explain them in brief. **[4]**

b) Write short note on complex programmable Logic Devices. **[4]**

c) Write verilog code for 4 bit ripple counter using four T-Flipflops. **[4]**

P.T.O.

Q4) Attempt any two of the following:

a) Draw the block diagram of 'Automatic Tablet Filling System'. Describe its working. **[6]**

b) i) A combinational logic is given by x=AB+ $A\overline{B} + \overline{A}\overline{B}$. Draw diagram of programmed PAL. **[3]**

ii) Describe Mealy model with block diagram. **[3]**

c) i) Explain in verilog multiway branching with example. **[3]**

ii) State 3 ways of specifying delays in continuous assignment statements and explain any one with example. **[3]**

OR

Q4) Answer all of the following.

a) Find the compatible state using merger graph **[4]**

Present State	Next State			
	00	01	10	11
A	C/0	–/–	A/0	–/–
B	–/–	E/0	B/0	D/1
C	D/0	B/1	–/–	–/–
D	C/0	A/1	E/0	–/–
E	B/0	–/–	A/0	E/1

b) Write short note on 'SPLD'. **[4]**

c) Explain continuous assignments statements in verilog. **[4]**

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