Total No. of Questions : 12]

SEAT No. :

P768

[Total No. of Pages : 3

# [4659] - 115

## B.E. (Electronics Engineering) (Semester - I)

## ADVANCED COMPUTER ARCHITECTURE

### (2008 Pattern) (Elective - II (a))

*Time : 3 Hours]* *[Max. Marks : 100*

***Instructions to the candidates:***

1) ***Answer any three questions from each section.***
2) ***Answers to the two sections should be written in separate books.***
3) ***Figures to the right indicate full marks.***
4) ***Assume suitable data, if necessary.***

## SECTION - I

***Q1)*** a) Why do we need high speed computing? Explain the Von-Neuman computer architecture and its limitations. **[8]**

b) What are performance metrics and measures used for parallel computers? Explain. **[8]**

c) What is cluster computing? **[2]**

OR

***Q2)*** a) What is speedup performance law? Explain Amdahl's law for speedup performance.

b) Discuss Flynn's classification of parallel computer architecture in detail.

c) Explain through put w.r.t. pipeline processing.

***P.T.O.***

*Q3)* a) What are the different types of hazards caused in the pipeline? How can these hazards be detected and resolved? **[8]**

b) Explain the following terms w.r.t. pipeline processing. **[8]**

i) Efficiency.

ii) Dynamic pipelining.

iii) Static pipelining.

iv) Internal forwarding.

OR

*Q4)* a) Compare superscalar & VLIW processor.

b) What do you mean by EPIC? State & explain features of EPIC.

*Q5)* a) State advantages of vector processing over scalar processing. **[8]**

b) Explain vector loop and pipeline chaining. **[8]**

OR

*Q6)* a) Explain the four types of vector instruction in Cray-1 in detail.

b) Explain the bottlenecks of vector processing.

## SECTION - II

*Q7)* a) What is inter - PE communications? Explain network design decisions for inter-PE communications. **[10]**

b) Discuss in detail static and dynamic topologies used in interconnection N/W. **[8]**

OR

*Q8)* a) State parallel algorithms for array processors. Explain in detail parallel sorting on array processor.

b) Explain cube interconnection network and hyper cube interconnection network.

***Q9)*** a) Explain loosely and tightly coupled multiprocessor system with example. **[8]**

b) Explain in detail chip multiprocessing. **[8]**

OR

***Q10)*** a) Write short note on:

i) Cross bar switch.

ii) Multiport memory.

b) Explain Cache coherancy and bus snooping.

***Q11)*** a) Discuss in brief latency hidding techniques. **[8]**

b) Explain : Data parallel programming techniques. **[8]**

OR

***Q12)*** a) Write short note on: **[8]**

i) Synchronous message passing.

ii) Asynchronous message passing.

b) Explain context switching overhead w.r.t. multithreading. **[2]**

c) Explain in detail shared memory programming. **[6]**