

Total No. of Questions : 10]

SEAT No. :

P3155

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[4858] - 1044

T.E. (E & TC)

Digital Signal Processing

(2012 Pattern) (End Sem.) (Semester - I)

Time : 2½ Hours]

[Max. Marks : 70

Instructions to the candidates:

- 1) Solve Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6, Q.7 or Q.8, Q.9 or Q.10.
- 2) Right side figures indicate marks.

- Q1)** a) Explain Advantages of Digital Signal Processing over Analog Signal Processing. [5]
- b) Explain the concept of orthogonality. [2]
- c) Check whether the functions given are orthogonal or not over an time interval $[0, 1]$ $f(t)=1; x(t)=\sqrt{3}(1-2t)$. [3]

OR

- Q2)** a) Compute 4-point DFT of sequence $x(n)=\{1,2,3,1\}$ using DIT-FFT radix-2 algorithm. What is Computational Complexity of Radix-2 FFT algorithm? [6]
- b) Compute circular convolution of $x_1(n)=\{1,2,3,4\}$ & $x_2(n)=\{2,1,2,1\}$. [4]

- Q3)** a) Plot the magnitude and phase spectrum of the sampled data sequence = $\{2, 0, 0, 1\}$ which was obtained using a sampling frequency of 20Hz. [5]
- b) Explain linear filtering effect for long duration sequences. [5]

OR

- Q4)** a) State any four properties of Z-Transform. [4]
- b) Compute Z-Transform and ROC of the following sequence

$$x(n)=\left[\frac{-1}{3}\right]^n u[n]-\left[\frac{1}{3}\right]^n u[-n-1]. \quad [6]$$

P.T.O.

- Q5) a)** Design a Butterworth filter using impulse invariant method transformation to satisfy the following specifications. [8]

$$0.707 \leq |H(e^{jw})| \leq 1 \quad \text{for } 0 \leq w \leq 0.2\pi$$

$$|H(e^{jw})| \leq 0.2 \quad \text{for } 0.6\pi \leq w \leq \pi$$

- b) Explain impulse invariant method for S-plane to Z-plane mapping. Explain its limitations. [8]

OR

- Q6) a)** What is frequency warping effect? How the mapping is done in bilinear transformation method? [7]

- b) Draw the direct form-I and II structures for the following systems. [9]

i) $3y(n) - 2y(n-1) + y(n-2) = 4x(n) - 3x(n-1) + 2x(n-2)$.

ii) $y(n) = 0.5[x(n) + x(n-1)]$.

- Q7) a)** Explain the characteristics of the FIR filters. [8]

- b) Determine the impulse response $h(n)$ of a filter having desired frequency response.

$$H_d(e^{jw}) = \begin{cases} e^{-j(N-1)w} & \text{for } 0 \leq |w| \leq \frac{\pi}{2} \\ 0 & \text{for } \frac{\pi}{2} \leq |w| \leq \pi \end{cases}$$

$N = 7$, use windowing technique approach. Use hamming window. [8]

OR

- Q8) a)** Explain Gibbs phenomenon. Compare between windows available. [8]

- b) Determine the impulse response $h(n)$ of a filter having desired frequency response,

$$H_d(e^{jw}) = \begin{cases} e^{-j(N-1)w} & \text{for } 0 \leq |w| \leq \frac{\pi}{2} \\ 0 & \text{for } \frac{\pi}{2} \leq |w| \leq \pi \end{cases}$$

$N = 7$, Use frequency sampling approach. [8]

- Q9)** a) What is sampling rate conversion? What is multirate DSP? Why it is required? [6]
- b) A signal $x(n)$, at a sampling frequency of 2.048 KHz is to be decimated by a factor of 32 to yield a signal at sampling frequency 64Hz. The signal band of interest extends from 0-30 Hz. The anti-aliasing filter should satisfy the following specifications:
- Pass Band deviation : 0.01dB
 Stop Band deviation : 80dB
 Pass Band : 0 – 30Hz
 Stop Band : 32 – 64Hz
- The signal components in the range from 30 to 32 Hz should be protected from aliasing. Design a suitable one-stage decimator. [8]
- c) How the DSP processors are selected? (any four points) [4]

OR

- Q10)** a) State four important features of DSP processors. [4]
- b) Draw the architecture of typical DSP processor TMS320C67XX and explain it in short. [6]
- c) 5 Design a two stage decimator that down samples an audio signal by a factor of 30, satisfying the following constraints: [8]
- Input sampling frequency : 240 KHz
 Highest frequency of interest : 3.4 KHz
 Passband ripple : 0.05
 Stopband attenuation : 0.01



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