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**[5152]-135****S.E. (Electronics & Telecommunication) (First Semester)****EXAMINATION, 2017****DIGITAL ELECTRONICS****(2012 PATTERN)****Time : Two Hours****Maximum Marks : 50****N.B. :-** (i) Figures to the right indicate full marks.

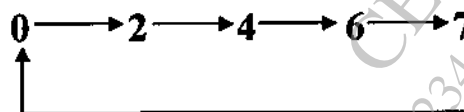
(ii) Neat diagrams must be drawn wherever necessary.

(iii) Assume suitable data, if necessary.

1. (a) Explain with neat diagram, interface of TTL gate driving CMOS gate and vice versa. [6]
- (b) Design a combinational circuit to produce the 2's complement of a 4 bit binary number as an input. [6]

*Or*

2. (a) Draw and explain the working of 2 input TTL NAND gate. [6]
- (b) Design even parity generator circuit for 4-bit input using multiplexer. [6]
3. (a) By using suitable flip-flop design a counter to go through the following states. Avoid lock out condition. [6]



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(b) Explain : [6]

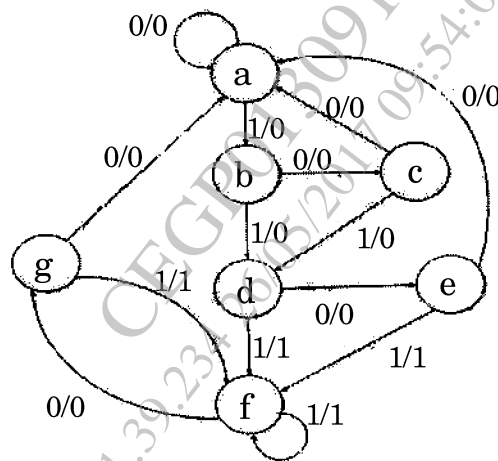
- (i) State Table
- (ii) State Diagram
- (iii) State Reduction.

Or

4. (a) Design a 3-Bit Binary Up/Down Ripple Counter. Draw the Timing Diagram. [5]

(b) For given state diagram (Figure given below) prepare State Table and reduce the same using 'State Table Reduction'.

[7]



5. (a) Explain in detail architecture of CPLD. [6]

(b) Implement the following functions using PLA : [7]

$$F_1(A, B, C) = \Sigma m(2, 3, 7)$$

$$F_2(A, B, C) = \Sigma m(3, 4, 6).$$

Or

6. (a) Explain difference between CPLD and FPGA. [5]

(b) Implement the following Boolean function using PAL : [8]

$$Y_1(A, B, C, D) = \Sigma m(1, 3, 4, 6, 9, 11, 12, 14)$$

$$Y_2(A, B, C, D) = \Sigma m(1, 3, 4, 6, 9, 11, 12, 14, 15)$$

$$Y_3(A, B, C, D) = \Sigma m(0, 2, 4, 6, 8, 12)$$

$$Y_4(A, B, C, D) = \Sigma m(2, 3, 8, 9, 12, 13)$$

7. (a) Explain the following Sequential Statements used in VHDL with suitable example : [8]

(i) If then Else statement

(ii) Case statement

(iii) Loop statement

(iv) Process statement.

(b) Write a VHDL code for JK Flip-Flop using asynchronous reset input. [5]

Or

8. (a) Explain the difference between concurrent statement and sequential statement in VHDL. [6]

(b) Write a VHDL code for 2-Bit comparator using behavioral modeling style. [7]