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**[4957]-1045**

**S.E. (E & TC/ Electronics) (First Sem.) EXAMINATION, 2016**  
**DIGITAL ELECTRONICS**  
**(2012 PATTERN)**

**Time : Two Hours****Maximum Marks : 50**

- N.B. :—** (i) Attempt Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6, Q.7 or Q.8.
- (ii) Neat diagrams must be drawn wherever necessary.
- (iii) Figures to the right indicate full marks.
- (iv) Assume suitable data, if necessary.
- (v) Use of logarithmic tables, slide rule and electronic non programmable calculator is allowed.

1. (a) Compare TTL & CMOS logic families on the basis of :[6]
- (i) Noise Margin
- (ii) Fan Out
- (iii) Propagation delay
- (iv) Figure of merit
- (v) Power supply voltage
- (vi) Switching speed.
- (b) Implement the following function using single 8 : 1 Multiplexer  
 $F(A,B,C,D) = \sum m(2,4,5,7,10,14)$  [6]

*Or*

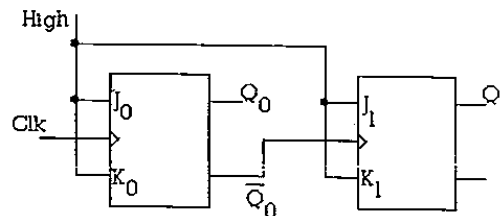
2. (a) Design a 2 bit magnitude comparator using suitable decoder. [6]
- (b) Design and explain the working of 2 input CMOS NAND Gate. [6]

P.T.O.

3. (a) Explain how shift registers are used as : [6]  
 (i) Ring counter  
 (ii) Twisted Ring counter.
- (b) Design and implement the following sequene generator using shift register .....1010..... [3]  
 Design mod-5 synchronous counter using T flip-flop. [3]

Or

4. (a) Design sequence detector to detect a sequence 1101 (Use D flip-flop and Mealy circuit) [6]  
 (b) For the ripple counter shown in figure show the complete timing diagram for eight clock pulses, showing the clock,  $Q_0$  and  $Q_1$  waveforms. [3]



- (c) What does the word 'Finite' signify in the terms finite state machine ? State advantages and disadvantages of a finite state machine. [3]
5. (a) Generate the following Boolean functions with a PAL with 4 inputs and 4 outputs. [3]

$$Y_3 = \overline{A}BC\overline{D} + A\overline{B}C\overline{D}$$

$$Y_2 = \overline{A}BC\overline{D} + \overline{A}BCD + ABCD$$

$$Y_1 = \overline{A}BC + A\overline{B}C + ABC\overline{D}$$

$$Y_0 = ABCD$$

- (b) Compare static RAMs and dynamic RAMs. [6]
- (c) Explain in brief the internal architecture of a PLA. [3]

*Or*

- 6. (a) Draw and explain  $8 \times 4$  bit PROM. [6]
- (b) (i) What is PLD ?
- (ii) State *two* advantages of PLD over fixed function IC and application specific IC.
- (c) State various characteristics of memory devices and explain in brief any *two*. [3]
- 7. (a) Write a VHDL code for 4-bit ALU with minimum 4 arithmetic and 4-logical operations using behavioral modeling. [6]
- (b) Give structural description of JK flip-flop. [4]
- (c) Compare if and case statements. [3]

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*Or*

- 8. (a) Write a VHDL code for 3-bit ripple down counter. [6]
- (b) What is difference between concurrent and sequential statements of VHDL. [4]
- (c) Give behavioral description of D flip-flop with Asynchronous Reset/Clear. [3]