

Total No. of Questions—8]

[Total No. of Printed Pages—3

Seat No.	
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**[5152]-163**

**S.E. (Computer Engineering)**  
**(First Semester) EXAMINATION, 2017**  
**DIGITAL ELECTRONICS AND LOGIC DESIGN**  
**(2012 PATTERN)**

**Time : Two Hours****Maximum Marks : 50**

**N.B. :—** (i) Attempt Q. No. 1 Or Q. No. 2, Q. No.3 Or Q. No. 4,  
 Q. No. 5 Or Q. No. 6, Q. No. 7 Or Q. No. 8.

(ii) Figures to the right indicate full marks.

(iii) Assume suitable data, if necessary.

1. (a) Do the required conversions for the following numbers. [6]

(i)  $(310.56)_{10} = ( )_2$

(ii)  $(5462)_8 = ( )_{16}$

(iii)  $(6516)_{10} = ( )_{16}$

(b) Define the following terms for TTL family : [2]

(i) Power dissipation

(ii) Speed of Operation.

(c) Explain two input CMOS NOR gate with neat diagram. [4]

Or

2. (a) Minimize the following functions using K-map and realize using logic gates.

$$F(A,B,C,D) = \sum m (1, 5, 7, 9, 11) \quad [4]$$

(b) Perform the following operation using 2's complement method

$$(35)_{10} - (18)_{10} = (?). \quad [2]$$

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- (c) Explain the working of three input TTL NAND gate with Totem pole output. [6]
3. (a) Implement the following function using 4 : 1 multiplexer  

$$F(A,B,C,D) = \sum m (1, 3, 7, 9, 11, 14, 15)$$
 [4]
- (b) Convert the following Gray code numbers to Binary : [2]
- (i)  $(101101)_2$
- (ii)  $(111111)_2$
- (c) What are the applications of FLIP- FLOPS ? Explain the working of JK Flip-Flop. [6]

*Or*

4. (a) Design four bit binary to gray code converter. Use logic gates as per your design and requirement. [6]
- (b) Design MOD 78 counter by using IC 7490 [6]
5. (a) What is VHDL ? Explain different modelling styles of VHDL with suitable example. [7]
- (b) What is ASM chart ? Explain components of ASM chart. What are applications of ASM chart in digital system design ? [6]

*Or*

6. (a) Draw an ASM chart and state table for 3-bit Up counter having control input E : [7]
- (i) If control input E = 0 : Counter remains in same state.
- (ii) If control input E = 1 : Counter goes to next state.
- (b) What is difference between signal and variable in VHDL ? Explain with an example. [6]
7. (a) Draw and explain the basic architecture of FPGA. [6]

(b) A combinational circuits is defined by the functions : [7]

$$F1 (A,B,C) = \sum m (0, 2, 5, 7)$$

$$F2 (A,B,C) = \sum m (0, 1, 6, 7)$$

Implement this circuit with PLA.

Or

8. (a) What is PLA ? Explain input buffer, AND and OR matrix in PLA. [7]

(b) What is CPLD ? Give the difference between CPLD and FPGA. [6]

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