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<b>Seat No.</b>	
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**S.E. (Computer Engineering)****EXAMINATION, 2014****DIGITAL ELECTRONICS AND LOGIC DESIGN****(2012 PATTERN)****Time : Two Hours****Maximum Marks : 50**

**N.B. :-** (i) Attempt Q. No. 1 or Q. No. 2, Q. No. 3 or Q. No. 4,  
Q. No. 5 or Q. No. 6, Q. No. 7 or Q. No. 8.

(ii) Figures to the right indicate full marks.

(iii) Assume suitable data, if necessary.

**1. (a) Do the following conversions : [6]**

(i)  $(1011.01)_2 \rightarrow ( \quad )_{10}$

(ii)  $(4C8.2)_{16} \rightarrow ( \quad )_{10}$

(iii)  $(0.6234)_{10} \rightarrow ( \quad )_8$

(b) What is logic family ? Give the classification of logic family. [3]

(c) Explain the wired logic output of TTL with neat diagram. [3]

P.T.O.

*Or*

2. (a) Minimize the following expression using Quine-McClusky : [6]

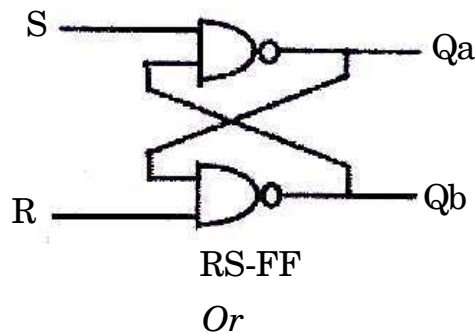
$$F(A, B, C, D) = \Sigma m (1, 5, 6, 12, 13, 14) + d(2, 4)$$

- (b) Explain with diagram 2 input CMOS NAND gate. [6]
3. (a) What do you mean by half adder and full adder ? How will you implement full adder using half adder ? Draw the circuit diagram. [6]
- (b) Explain with neat diagram working of parallel in serial out 4-bit shift register. Draw necessary timing diagram. [6]

*Or*

4. (a) Explain in detail Look Ahead Carry generator. [6]
- (b) Design a MOD-5 synchronous counter using JK FF and implement it. Also draw timing diagram. [6]
5. (a) Draw the ASM chart for the following state machine. A 2-bit up counter is to be designed with output Q, Q0, and enable signal 'X'. If X = 0, then counter changes the state as 00 – 01 – 10 – 11 – 00. If 'X' = 1 then counter remains in same state. Design the circuit using JK-FF and suitable MUX. [7]

- (b) What is meant by Entity and Architecture in VHDL ? Write the architecture of RS FF as given below in structural modeling. Assume entity NAND 2 A, B input and Y output. [6]



- (a) Write VHDL code for 2-bit comparator circuit. Use behavioural modeling style. [6]
- (b) Draw an ASM chart and state table for a 2-bit Up-Down counter having mode control input M
- When  $M = 1$  : UP counting
- When  $M = 0$  : Down Counting
- The circuit should generate output whenever counter becomes minimum or maximum. [7]
7. (a) What do you mean by FPGA ? Explain the internal architecture of FPGA. State the importance of configurable logic block in FPGA. [7]
- (b) What is PLA ? Explain the input buffer AND and OR Matrix in PLA. [6]

Or

8. (a) Implement the following Boolean function using PAL : [7]

$$W(A, B, C, D) = \Sigma m (0, 2, 6, 7, 8, 9, 12, 13)$$

$$x(A, B, C, D) = \Sigma m (0, 2, 6, 7, 8, 9, 12, 13, 14)$$

$$y(A, B, C, D) = \Sigma m (2, 3, 8, 9, 10, 12, 13)$$

$$z(A, B, C, D) = \Sigma m (1, 3, 4, 6, 9, 12, 14)$$

- (b) A combinational circuit is defined by the function : [6]

$$F1 = \Sigma m(3, 5, 7)$$

$$F2 = \Sigma m(4, 5, 7)$$

Implement the circuit with PLA having 3 input and 3 product term with 2 output.